1. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate; and

a multi-layered wiring arrangement provided on said semiconductor substrate, said multi-layered wiring arrangement including at least one insulating layer structure having a metal wiring constitution formed therein,

wherein said insulating layer structure includes a first SiOCH layer, a second SiOCH layer formed on said first SiOCH layer, and a silicon dioxide (SiO_2) layer formed on said second SiOCH layer, and said second SiOCH layer features a carbon (C) density lower than that of said first SiOCH layer, a hydrogen (H) density lower than that of said first SiOCH layer, and an oxygen (O) density higher than that of said first SiOCH layer.

2. (Original) A semiconductor device as set forth in claim 1, wherein said first SiOCH layer features the carbon (C) density falling in a range between 10 atoms % and 20 atoms %, the oxygen (O) density falling in a range between 20 atoms % and 35 atoms %, and the hydrogen (H) density of more than 25 atoms %, and said second SiOCH layer features the carbon (C) density of less than 10 atoms %, the oxygen (O) density of more than 35 atoms %, and the hydrogen (H) density of less than 25 atoms %.

3. (Original) A semiconductor device as set forth in claim 1, wherein said insulating layer structure has a trench pattern formed therein, and said metal wiring constitution comprises a metal wiring pattern buried in said trench pattern.

4. (Original) A semiconductor device as set forth in claim 3, wherein said metal wiring pattern is made of copper (Cu), and a barrier metal layer is formed on wall faces defining said trench pattern to thereby prevent diffusion of copper atoms from said copper

wiring pattern into said insulating layer structure.

5. (Original) A semiconductor device as set forth in claim 4, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

6. (Original) A semiconductor device as set forth in claim 5, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

7. (Original) A semiconductor device as set forth in claim 4, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

8. (Original) A semiconductor device as set forth in claim 7, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

9. (Original) A semiconductor device as set forth in claim 4, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

10. (Original) A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

11. (Original) A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer and a SiCH layer.

12. (Original) A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

13. (Original) A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

14. (Original) A semiconductor device as set forth in claim 4, wherein said copper wiring pattern contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

15. (Original) A semiconductor device as set forth in claim 1, wherein said insulating layer structure has at least one hole formed therein, and said metal wiring constitution comprises a metal via-plug buried in said hole.

16. (Original) A semiconductor device as set forth in claim 15, wherein said metal via-plug is made of copper (Cu), and a barrier metal layer is formed on wall faces defining said hole to thereby prevent diffusion of copper atoms from said copper via-plug

into said insulating layer structure.

17. (Original) A semiconductor device as set forth in claim 16, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

18. (Original) A semiconductor device as set forth in claim 17, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

19. (Original) A semiconductor device as set forth in claim 16, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

20. (Original) A semiconductor device as set forth in claim 19, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

21. (Original) A semiconductor device as set forth in claim 16, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

22. (Original) A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

23. (Original) A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer and a SiCH layer.

24. (Original) A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

25. (Original) A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

26. (Original) A semiconductor device as set forth in claim 16, wherein said copper via-plug contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

CLAIMS 27-82 (CANCELLED)

83. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate; and

a multi-layered wiring arrangement provided on said semiconductor substrate, said multi-layered wiring arrangement including at least one insulating layer structure having a metal wiring constitution formed therein,

wherein said insulating layer structure includes a first SiOCH layer, a second SiOCH layer formed on said first SiOCH layer, and a silicon dioxide (SiO_2) layer formed on said second SiOCH layer, and said second SiOCH layer features a carbon (C) density lower than that of said first SiOCH layer, a hydrogen (H) density lower than that of said first SiOCH layer, and an oxygen (O) density higher than that of said first SiOCH layer. wherein said first SiOCH layer features the carbon (C) density falling in a range between 10 atoms % and 20 atoms %, the oxygen (O) density falling in a range between 20 atoms % and 35 atoms %, and the hydrogen (H) density of more than 25 atoms %, and said second SiOCH layer features the carbon (C) density of less than 10 atoms %, the oxygen (O) density of more than 35 atoms %, and the hydrogen (H) density of less than 25 atoms %.

84. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate; and

a multi-layered wiring arrangement provided on said semiconductor substrate, said multi-layered wiring arrangement including at least one insulating layer structure having a metal wiring constitution formed therein,

wherein said insulating layer structure includes a first SiOCH layer, a

second SiOCH layer formed on said first SiOCH layer, and a silicon dioxide (SiO_2) layer formed on said second SiOCH layer, and said second SiOCH layer features a carbon (C) density lower than that of said first SiOCH layer, a hydrogen (H) density lower than that of said first SiOCH layer, and an oxygen (O) density higher than that of said first SiOCH layer, wherein said insulating layer structure has a trench pattern formed therein, and said metal wiring constitution comprises a metal wiring pattern buried in said trench pattern, wherein said metal wiring pattern is made of copper (Cu), and a barrier metal layer is formed on wall faces defining said trench pattern to thereby prevent diffusion of copper atoms from said copper wiring pattern into said insulating layer structure, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution, wherein said barrier insulating layer has a multi-layered structure selected from the group comprising one of (a) a SiCNH layer and a SiCH layer, (b) a SiCNH layer, and a SiOCNH layer formed thereon, and (c) a SiCNH layer, and a SiCH layer formed thereon.

85. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate; and

a multi-layered wiring arrangement provided on said semiconductor substrate, said multi-layered wiring arrangement including at least one insulating layer structure having a metal wiring constitution formed therein,

wherein said insulating layer structure includes a first SiOCH layer, a second SiOCH layer formed on said first SiOCH layer, and a silicon dioxide (SiO_2) layer

formed on said second SiOCH layer, and said second SiOCH layer features a carbon (C) density lower than that of said first SiOCH layer, a hydrogen (H) density lower than that of said first SiOCH layer, and an oxygen (O) density higher than that of said first SiOCH layer, wherein said insulating layer structure has at least one hole formed therein, and said metal wiring constitution comprises a metal via-plug buried in said hole, wherein said metal via-plug is made of copper (Cu), and a barrier metal layer is formed on wall faces defining said hole to thereby prevent diffusion of copper atoms from said copper via-plug into said insulating layer structure, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution, wherein said barrier insulating layer has a multi-layered structure comprising one of (a) a SiCNH layer and a SiCH layer, (b) a SiCNH layer, and a SiOCNH layer formed thereon, (c) a SiCNH layer, and a SiCH layer formed thereon.

86. (New) A semiconductor device as set forth in claim 1, wherein said second SiOCH layer has a smaller thickness than that of said first SiOCH layer.

87. (New) A semiconductor device as set forth in claim 83, wherein said second SiOCH layer has a smaller thickness than that of said first SiOCH layer.

88. (New) A semiconductor device as set forth in claim 84, wherein said second SiOCH layer has a smaller thickness than that of said first SiOCH layer.

89. (New) A semiconductor device as set forth in claim 85, wherein said second SiOCH layer has a smaller thickness than that of said first SiOCH layer.